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## Abstract

AC coupled silicon detectors, being used for the D0 upgrade, may have substantial voltage across the coupling capacitor. Failed capacitors can present  $\sim 50$  V to the input of the SVX, Silicon Vertex, device. We measured the effects that failed detector coupling capacitors have on the SVXD (rad soft  $3\mu\text{m}$ ), SVXH (rad hard  $1.2\mu\text{m}$ ), and SVXIIB (rad soft  $1.2\mu\text{m}$ ) amplifier / readout devices. The test results show that neighboring channels saturate when an excessive voltage is applied directly to a SVX channel. We believe that the effects are due to current diffusion within the SVX substrate rather than surface currents on the detectors. This paper discusses the magnitude of the saturation and a possible solution to the problem.

## I. INTRODUCTION

The D0 Central Tracking Upgrade includes replacing the Vertex Detector with an array of single and double sided 50 micron pitch silicon detectors. The double sided detectors will have one half of the depletion voltage across each coupling capacitor. In the event that this capacitor fails, the detector's bias voltage is applied directly to the corresponding input buffer of the SVX device via a polysilicon 2 Megohm bias resistor. We simulate a failed capacitor by directly connecting a power supply to the chip input through a 2 Megohm resistor. Data is presented for both positive and negative bias voltages applied to three types of SVX integrated circuit technologies.

## II. ISOLATED SVX MEASUREMENTS

### A. Procedure

Figure 1 shows the schematic of a silicon detector channel and the front end buffer of a SVX. During these tests the silicon detector is replaced with a 2 Megohm resistor, simulating a failed capacitor. As the input voltage applied to a single channel of the SVX device is incremented, the voltage at the input to the buffer (probe voltage) and the output counts of several neighboring channels were recorded. The channel receiving this voltage directly is known as the seed channel. Channels which are adjacent to the seed channel are referred to as neighbors.

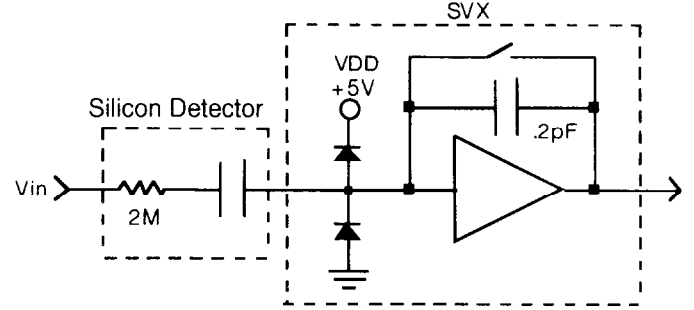


Figure 1: Silicon Detector and SVX Schematic

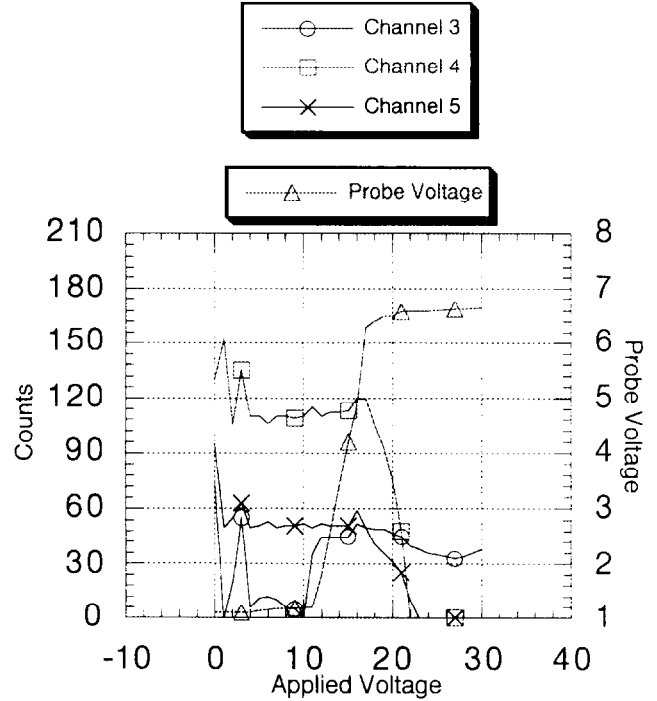


Figure 2: SVXD Neighbor Channel Saturation

### B. SVXD Results

The first version of the SVX to be produced was the SVXD. This device was made by Hewlett Packard with rad soft  $p$ -well  $3\mu\text{m}$  technology. Figure 2 shows that as positive voltage is applied to the seed (channel 3) neighboring channels 4 and 5 saturate. Saturation effects were also seen on channels 6 and 7 which are not shown for clarity. The Y axis, on the right side of the graph, shows the probe voltage. The output of the neighboring channels begins decreasing as the protection

diode reaches the clamping voltage. Saturation is indicated by a decrease in the output counts. When a negative voltage is applied to the seed, the saturation effect is not seen.

### C. SVXH Results

The second version of the SVX was produced by United Technologies Microelectronics Center (UTMC) with rad hard  $1.2\mu\text{m}$   $p$ -well technology. Figure 3 shows the declining output of first neighbor channels when the voltage applied to the seed (channel 95) increases. The plot shows that after the seed channel saturates and the protection diode reaches the clamping voltage, neighboring channels start to saturate. Saturation is indicated by lower output count values. Second and third neighbor channels also exhibit saturation as the input voltage to the seed channel increases. The saturation effect does not occur to neighboring channels when negative voltage is applied to the seed channel.

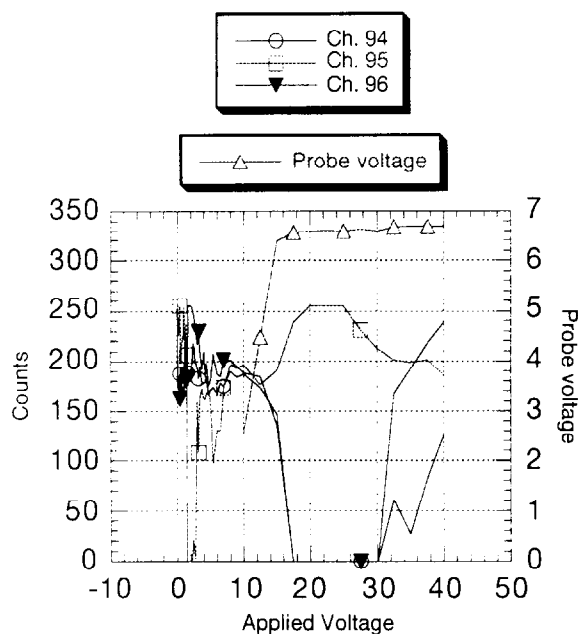


Figure 3: SVXH First Neighbor Saturation

### D. SVXIIB Results

The most recent version of the SVX, SVXIIB, is produced by Hewlett Packard with rad soft  $n$ -well  $1.2\mu\text{m}$  technology. Figure 4 shows that as positive voltage is applied to the seed (channel 62) the neighboring channels do not saturate. An externally generated pulse was applied to the first neighbor channels during this test. The output counts of the pulsed channels remains constant at 200 counts while the voltage applied to seed was increased. The seed output reaches a peak of 255 counts when  $.316\mu\text{A}$  is applied to the buffer. Seed current of  $1.77\mu\text{A}$  causes the output to decrease to a baseline of 40 counts. Second neighbor channel outputs remain at 40 counts throughout the test.

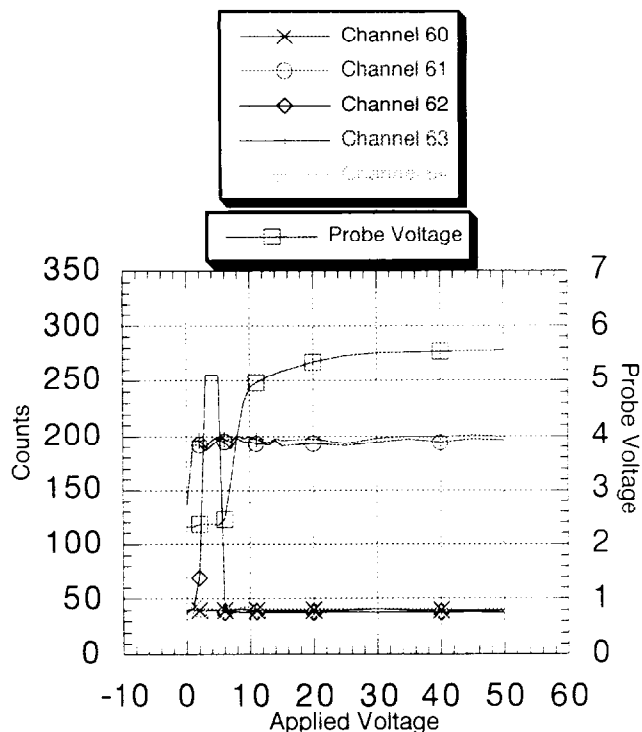


Figure 4: SVXIIB Normal Operation

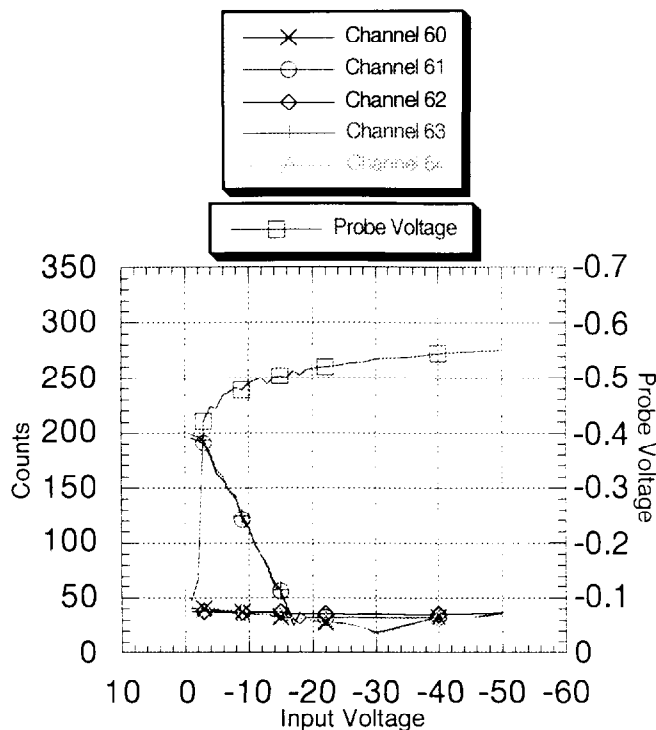


Figure 5: SVXIIB Neighbor Channel Saturation

Figure 5 shows that as negative voltage is applied to the seed, the output of the first neighbor channels decreases from 200 counts to a baseline value of approximately 40 counts.

The output counts of the second neighbor channels decrease to 18 counts, however, they tend to gradually increase to the baseline level of 40 counts. Saturation is again indicated by lower output counts. The probe voltage curve again shows that as the diode begins to conduct, neighbor channels start to become affected.

### III. LINEAR SATURATION RESPONSE

The amount of seed current required to cause neighbor channels to saturate can be calculated from the probe voltage measurement. Figure 6 shows the amount of seed current needed for saturation to occur in the SVX chips. As the amount of seed current increases, the number of channels affected also increases. Saturation effects were not seen on third neighbor channels of the SVXIIB chip.

VERSION	CURRENT	NEIGHBOR
SVXD	7.7 $\mu$ A	First
	8.2 $\mu$ A	Second
	10.2 $\mu$ A	Third
SVXH	5.47 $\mu$ A	First
	9.20 $\mu$ A	Second
	14.2 $\mu$ A	Third
SVXIIB	8.24 $\mu$ A	First
	14.7 $\mu$ A	Second

Figure 6: Neighbor Saturation Current

Figure 7 shows the linear relationship between the amount of seed current required for saturation to occur and the corresponding neighbor channel for the SVXH chip. This plot tells us that as the distance from the seed channel increases, the current required to cause saturation also increases. The distance between each channel is 50  $\mu$ m. The test results show that approximately 100nA/ $\mu$ m is required to cause saturation.

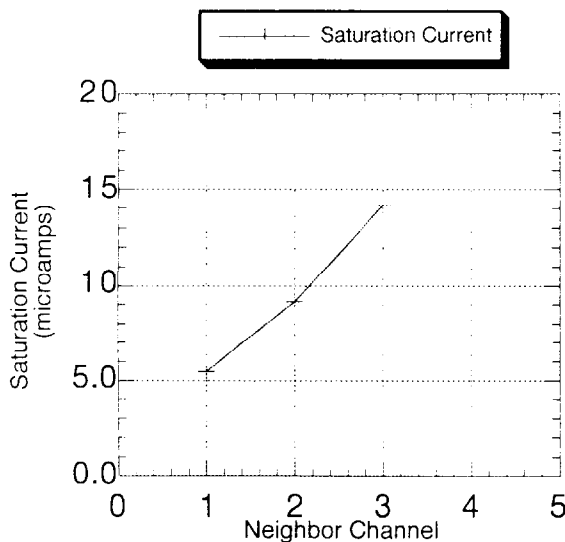


Figure 7: Saturation Current VS Neighbor Channel

### IV. SVX TECHNOLOGIES

The cause of the saturation effect can be linked to the type of technology used to produce the SVX devices. The test results show that *p*-well devices saturate when positive voltage is applied to a seed channel. Neighboring channels on *n*-well devices saturate when negative voltage is applied to the seed channel. Figures 8 and 9 show how the SVX buffer protection diodes are constructed for *p*-well and *n*-well technologies.

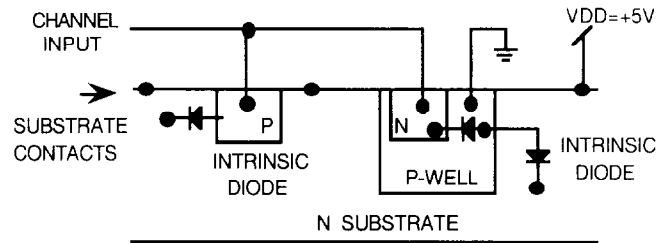


Figure 8: SVXD and SVXH *p*-well Technology

Substrate surface contacts are represented as black dots. The channel input is connected to the *p*-type dopant and the *p*-well *n*-type dopant. The protection intrinsic diode is formed between the *p*-type dopant and the *n*-type substrate. The well protection diode is formed between the *n*-type dopant and the *p*-well. A surface contact connects the *p*-well to ground. Another intrinsic diode is formed between the *p*-well and the *n*-type substrate. This diode is not considered part of the protection circuit. The reference voltage (VDD) is connected by several surface contacts.

The current path for *p*-well devices, when negative voltage is applied to an SVX channel, is through the *p*-well diode to ground. However, when an excessive positive voltage is applied, the intrinsic diode formed by the *p*-type dopant and the *n*-type substrate conducts. When this intrinsic diode conducts, saturation occurs on neighboring channels.

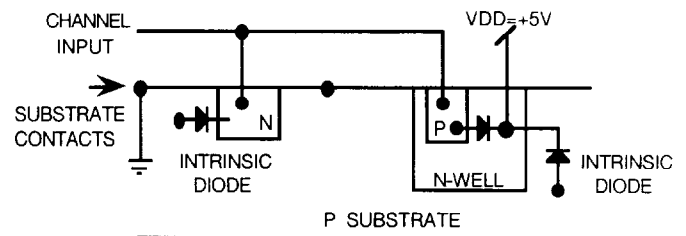


Figure 9: SVXIIB *n*-well Technology

The operation of the *n*-well technology is similar to that of the *p*-well technology except that the intrinsic protection diode conducts when an excessive negative voltage is applied to a channel. The substrate surface contacts for the *n*-well technology are at ground potential and the diode reference voltage is connected to the *n*-well of the protection diode.

To understand how saturation of neighboring channels occurs, one needs to visualize the relationship between adjacent channel intrinsic protection diodes. Figure 10 shows the components of an intrinsic transistor formed with *n*-well technology.

The forward biased base-emitter junction is formed by the intrinsic protection diode of the seed channel. The reverse biased base-collector junction is formed by the intrinsic protection diode associated with the first neighbor channel. The base is formed by the substrate of the chip. The *p*-well technology produces a PNP intrinsic transistor whereas the *n*-well technology produces a NPN intrinsic transistor.

As the negative voltage applied to the SVXIIb seed channel increases, the intrinsic protection diode of the seed channel conducts and emits electrons into the substrate. The base-collector junction is reversed biased due to the static condition of neighboring channels. Transistor action occurs which causes electrons to be emitted from the collector and directly into the buffer of the neighboring channel.

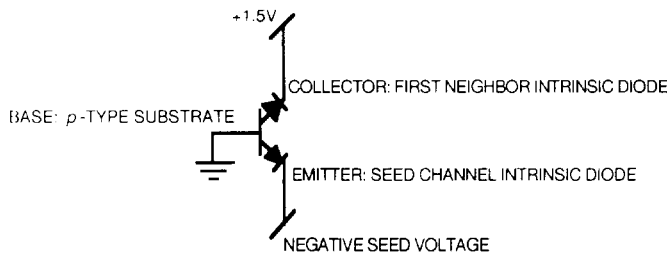


Figure 10: *n*-well Technology Intrinsic Transistor

To test the intrinsic transistor hypothesis, a SVXIIb channel was modified by cutting the protection diodes out of the circuit and placing a jumper from the input bonding pad directly to the input of the buffer. Figure 11 shows the result of removing the protection diodes associated with channel 44. Channel 45 is the seed channel. As negative voltage is applied to the seed channel, the first neighbor (channel 46) saturates. Channel 44 does not saturate since the diodes have been removed. The absence of a channel's protection diodes caused a first neighbor to saturation at a lower applied seed voltage because more current was available. This increase in available current also caused the second neighbor channel (channel 43), located next to the modified channel, to saturate first. Earlier data reveals that symmetrical neighbors about the seed saturate at the same applied seed voltage. This test proves that the intrinsic transistor action exists.

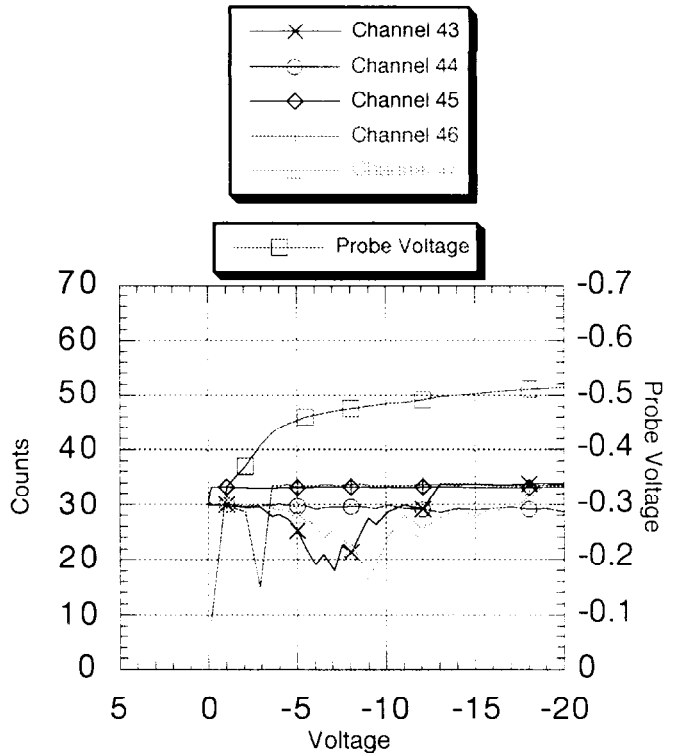


Figure 11: SVXIIb - Modified Channel 44

## V. CONCLUSION

Three versions of the SVX chip have been tested. Each version exhibits neighboring channel saturation effects when intrinsic protection diodes conduct. Tests have been completed which confirms that intrinsic transistors are formed between the protection diodes of adjacent channels. We intend to increase the distance between the diodes in the next version of the chip to eliminate the problem.

## VI. ACKNOWLEDGMENTS

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